A first evaluation of thick oxide 3C-SiC MOS capacitors reliability

Fan Li, Qiu Song, Amador Perez-Tomas, Vishal Shah, Yogesh Sharma, Dean Hamilton, Craig Fisher, Peter Gammon, Mike Jennings, and Phil Mawby

***Abstract*— Despite the recent advances in 3C-SiC technology, there is a lack of statistical analysis on the reliability of SiO_2 layers on 3C-SiC, which is crucial in power MOS device developments. This paper presents a comprehensive study of the medium and long-term time-dependent dielectric breakdown (TDDB) of 65 nm thick SiO_2 layers thermally grown on a state-of-the-art 3C-SiC/Si wafer. Fowler-Nordheim (F-N) tunnelling is observed above 7 MV/cm and an effective barrier height of 3.7 eV is obtained, which is highest known for native SiO_2 layers grown on the semiconductor substrate. The observed dependence of the oxide reliability on the gate active area suggests the oxide quality has not reached the intrinsic level. Three failure mechanisms were identified, confirmed by both medium and long-term results. Whereas two of them are likely due to extrinsic defects from material quality and fabrication steps, the one dominating the high field (>8.5 MV/cm) should be attributed to the electron impact ionization within SiO_2. At room temperature, the field acceleration factor is found to be ≈0.906 dec/ (MV/cm) for high fields, and the projected life-time exceeds 10 years at 4.5 MV/cm.**

***Index Terms*— Reliability, 3C-SiC, MOS capacitor, TDDB, failure mechanism.**

I. Introduction

SILICON CARBIDE (SiC) can provide better electrical performance than Si in more harsh operation conditions (high power, high frequency and high temperature), thus have been considered as the next generation substrates for power devices. 4H-SiC Schottky barrier diodes (SBD), JFETs, and MOSFETs are commercially available now. The 4H-SiC SBDs proved to be a success in boost converters, whereas the switches (JFETs or MOSFETs) have not been widely accepted as their Si counterparts.

Compared with other wide band gap (WBG) semiconductors, SiC has the advantage that SiO_2 layers can be directly thermally grown on the epilayer as the gate dielectric for MOS devices. The reliability of this SiO_2 layer is a major attribute of a MOSFET development and the required lifetime of power electronics systems can reach up to 30 years [1], thus gate dielectrics are expected to have a similar lifetime. In the early days of the Si industry, the SiO_2 on Si system was intensively studied and is now well developed compared with investigations performed on 4H-SiC [2-12]. Even now, the gate oxide reliability of large active 4H-SiC MOS devices (5-50 mm^2) is still not as good as the early Si devices with comparable gate oxide area [13]. Regardless, in the last decade, a great improvement of the lifetime of SiO_2 on 4H-SiC has been seen, from below 1000 s (6 MV/cm, 350 °C) [3] to most recently 2300 h (6 MV/cm, 250 °C) [6]. Yet it was believed impossible to reach the stability of the Si/SiO_2 interface, due to an inherent smaller conduction bands offset ΔE_C between 4H-SiC and SiO_2 [4]. In the high field condition, the oxide intrinsic degradation is believed to be dominated by F-N tunnelling [14], and the affinity difference at the semiconductor/oxide interface is the potential barrier Φ_B for such tunnelling. In a strong inversion case such as the MOSFET being switched on, $\Phi_B \approx \Delta E_C$ [4]. The theoretical value of ΔE_C for 4H-SiC/SiO_2 is 2.7 eV and had recently been experimentally reported [15], whereas the value for Si is 3.2 eV, and for 3C-SiC 3.7 eV [16], potentially the most stable among the three. Moreover, the smaller bandgap means most of the traps troubling the 4H-SiC/SiO_2 interface are located in the conduction band of 3C-SiC, namely not contributing to degrade the channel mobility, thus lower channel resistance for a MOSFET. 3C-SiC technology is not yet as popular as 4H-SiC, mainly due to the lack of device grade, high quality 3C-SiC substrates. However, the ability to deposit 3C-SiC on large area Si wafers (6-inch 3C-SiC on Si wafers demonstrated 20 years ago [17]) makes it attractive in terms of cost-effective. In the last ten years, there have been many improvements in 3C-SiC substrate preparation [18-24] that a defect density below 400 cm^{-1} became possible [24]. There were also further developments in 3C-SiC device processing, including implantation [25, 26], oxidation [27-29], and metallisation [30, 31]. 600 V vertical power MOSFET was demonstrated with a specific on-resistance of 8.2 $m\Omega.cm^2$ [32].

Regarding the 3C-SiC/SiO_2 interface, some study was performed on the interface trap density [33, 34] and channel mobility [29, 35, 36], whereas very little on the reliability. In

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[16], dielectric breakdown of very thin (6-7 nm) and small area (100 nm diameter) thermally grown SiO_2 on 3C-SiC(111) was studied by Time Dependent Dielectric Breakdown (TDDB) test at 10 V (≈15 MV/cm), and Weibull slope β values of 4.4-5.1 were obtained. This is close to the performance of SiO_2 layers on Si with similar thickness. However, for thin oxides the leakage current stays almost constant until failure, which is in contrast to thick oxides, where electron/hole trapping cause the current level to change a lot during stress [14]. Since the tunnelling current generates defects in the oxide, leading to their eventual degradation [4], thin and thick SiO_2 layers tend to have different failure mechanisms. Also, under the same electric field, carriers in thicker oxides are more likely to gain a higher energy for impact ionization [9], which is often considered as another potential cause of oxide failure. Practical power devices usually have thick (>50 nm) SiO_2 layer in order to sustain the gate voltage [4, 7]. To the best of our knowledge, the reliability of thick SiO_2 on 3C-SiC has not been reported.

In this paper, 3C-SiC MOS capacitors were fabricated with ≈65 nm thermally grown SiO_2 layers as the gate dielectric. I-V characterisation was used to study the effective barrier height at the 3C-SiC/SiO_2 interface. Medium-term test lasting weeks was then performed and the failure distribution was obtained for a wide electric field range of 4.5-10.5 MV/cm. Following the medium-term results, long-term TDDB tests lasting months were conducted for 6, 7.5, 8.5 and 9 MV/cm. All characterisations were performed at room temperature. Based on the failure distribution and TDDB plots, Weibull models were used to predict the fabricated MOS capacitors failure rate and lifetime.

II. Experimental

10 µm thick unintentionally doped (<1×10^{16} cm^{-3}) N-type 3C-SiC(100) layers were epitaxy grown on-axis from a 4-inch Si(100) substrate. The as-grown 3C-SiC epilayer was treated with a chemical mechanical polishing (CMP) step in order to obtain a low surface root mean square roughness ≈0.2 nm, measured by atomic force microscopy (AFM). Since it is the 3C-SiC/SiO_2 interface that is of interests here, lateral MOS capacitors were fabricated in order to minimize the disturbing electrical effects from the 3C-SiC/Si heterojunction. For ohmic contact, nitrogen was selectively implanted to form a 300 nm deep box profile with the peak concentration of ≈5×10^{20} cm^{-3}, and a post implantation anneal was performed at 1350 ºC for 2 hours in Ar atmosphere. No surface capping layer had been used during the post implantation anneal. Our previously study [26] shows that, this will lead to a ≈15% activation of the implanted nitrogen dopants. After the post implantation anneal, solvent cleans were performed (acetone, propanol, acetone, and methanol, each step 5 mins) in an ultrasonic bath. Following that, a two-stage acid clean was applied, first piranha (H_2SO_4:H_2O_2=3:1, 15 mins) then RCA (RCA1 15 mins+ RCA2 15 mins). A 2 µm thick SiO_2 layer was deposited via low pressure chemical vapour deposition as the surface passivation dielectric. Photo lithography and reactive ion etching (RIE) was used to selectively etch the deposited 2 µm SiO_2 down to the 3C-SiC surface, where the gate thermal oxidation occurred. Dry oxidation (1200 ºC, 10 mins, 1 slm O_2) followed by a post oxidation anneal in N_2O (1200 ºC, 120 mins, 1 slm N_2O) was performed to obtain the gate oxide. The final gate oxide was around 65 nm thick, measured by the ellipsometry. AFM evaluations of the 3C-SiC surface morphology after post implantation anneal [26] and thermal oxidation [27] had been shown in our previous reports that, no significant roughness degradations were observed. Ohmic metallisation was obtained by RIE etching the passivation oxide and evaporating firstly a 30 nm Ti layer then a 100 nm Ni layer on the N+ regions. A rapid thermal anneal at 1000 ºC for 2 mins in Ar was performed to form the ohmic contact with specific contact resistance below 1×10^{-5} Ω.cm^2 [31]. Finally, the gate contact was defined by selectively evaporating 500 nm thick Al above the gate oxide region. The final device has a circular gate active area, and a cross section view of the structure is shown in Fig. 1. MOS capacitors with three gate diameters were fabricated, namely Φ100 µm, Φ200 µm and Φ400 µm.

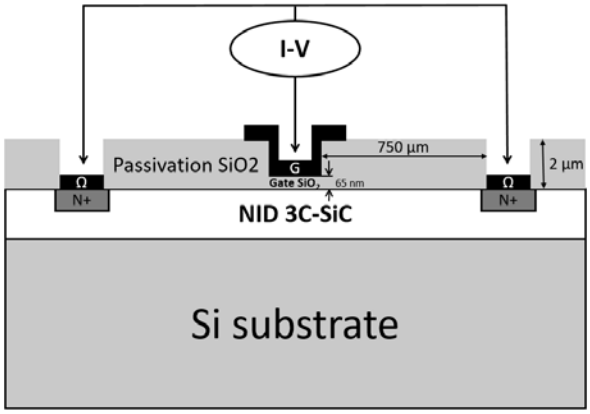

Fig. 1. A schematic cross section view of the fabricated circular lateral 3C-SiC MOS capacitors, dimensions are not to scale.

III. Results and Discussions

A. Capacitance-voltage (C-V) characterisation

Room temperature C-V (1 kHz and 1 MHz) characterisations were performed on these MOS capacitors using a LCR meter. A negative flat band voltage was observed as shown in Fig. 2, which is also commonly reported in the literature [32, 36, 37]. It is generally believed to be caused by the nature of donor-like states at the 3C-SiC/SiO_2 interface, which have a lower density than 4H-SiC but are positively charged [38]. The effective fixed charge density was calculated to be around 2.1×10^{12} cm^{-2} according to the flat band shift from the ideal value. This value is typical among lately reported results [16, 28]. Using the high-low method [39], the interface trap density at 0.2 eV from the 3C-SiC conduction band edge was extracted to be 2.5×10^{11} $cm^{-2}eV^{-1}$, which is among the lowest values reported in recent literatures [28, 34, 40].

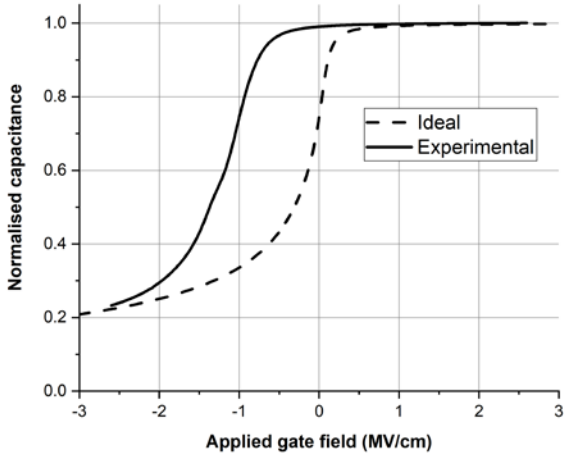

Fig. 2. Experimental (1 MHz) and ideal C-V characterisations of the fabricated lateral MOS-C.

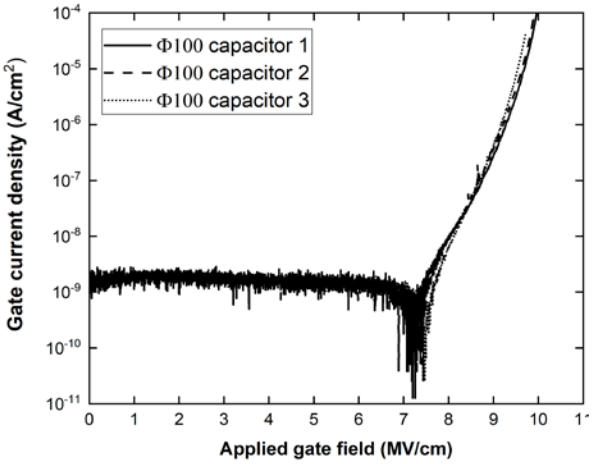

Fig. 3. Representative gate leakage current densities as a function of the electric field in the oxide for the Φ100 MOS capacitors.

B. Dielectric breakdown and F-N tunnelling

By performing room temperature I-V measurements using a Keysight B1500 parameter analyser, the leakage current density of Φ100 devices as a function of the electric field in the oxide is obtained and shown in Fig. 3. As can be seen in Fig. 3, when the electric field reaches ≈7 MV/cm, the gate leakage current density becomes dominated by F-N tunnelling, which usually comes into effect at a lower electric field of 5-5.5 MV/cm for 4H-SiC MOS gate oxides [7-12, 15]. The effective barrier height Φ_B can be obtained by fitting the linear region of the experimental "$\ln(J/E_{ox}^2)$ vs $1/E_{ox}$" plot to the following expression [15]:

$$\ln\left(\frac{J}{{E_{ox}}^2}\right) = \frac{q^3\left(\frac{m_0}{m_{ox}}\right)}{8\pi h\Phi_B} - \frac{8\pi\sqrt{2m_{ox}{\Phi_B}^3}}{3qhE_{ox}} \quad (1)$$

where J is the gate leakage current density, E_{ox} is the electric field within the gate oxide, m_0 is the free electron mass, m_{ox}=0.42m_0 [41] is the effective electron mass, q is the unit electron charge, and h is the Plank constant. The experimental effective barrier height Φ_B was obtained as 3.65-3.71 eV for the representative results shown in Fig. 3, approaching the theoretical value of 3.7 eV.

C. Medium-term reliability and failure distribution

We investigated the failure distribution of these MOS capacitors in a wide field range of 4.5-10.5 MV/cm. For each studied electric field, the gate bias V_G was kept constant for 1 hour before increasing to the next value. More details about this method can be found in [1].

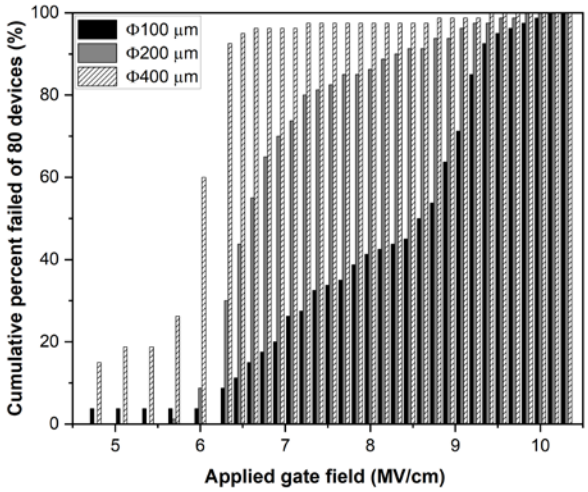

Fig. 4. The failure distribution of Φ100, Φ200 and Φ400 MOS capacitors in the electric field range of 4.5-10.5 MV/cm.

For each gate diameter, 80 MOS capacitors were tested. As can be seen in Fig. 4, the failure distribution varies considerably with the gate diameter that, larger devices tend to fail more easily than smaller ones as the gate bias elevates. Similar area dependence was observed also in 4H-SiC TDDB results (area of 100×100-200×800 μm^2) [7]. At least three mechanisms are recognisable from the failure distribution of the Φ100 MOS capacitors. Neglecting the 3 premature failures at 4.5 MV/cm, it can be seen that between 6 MV/cm and 7.5 MV/cm, the number of failures accumulate gradually. In this low field range, failure is crucially determined by the number of extrinsic defects per device (namely gate active area) and defined as mechanism I. From the literature, these first priority defects may be pre-existing basal plane dislocations in the 3C-SiC epilayer [42], or local step-bunching edges where dielectric break down can be accelerated [16]. Reaching 7.5 MV/cm, it seems that almost all mechanism I failures have occurred, and the increase of total failure number slows down, suggesting a new mechanism II becoming dominant. Mechanism II induced failures have a much smaller increase rate against elevating electric fields (more obviously shown later in Fig. 5), thus can be easily overshadowed by other mechanisms. The cause of mechanism II could be the extrinsic defects created during the device fabrication or a relatively high stacking fault density in the 3C-SiC epilayer. Above 8.5 MV/cm, a considerably sharp increase of the total failed devices is observed, namely mechanism III. It is worth mentioning that 8.5-9 MV/cm is also previously reported in 4H-SiC TDDB tests as a juncture point where the failure mechanism changes [7-9]. For 4H-SiC, one of the common explanations for such change at high electric fields is F-N tunnelling. As mentioned previously, F-N tunnelling

almost always occurred around 5-5.5 MV/cm in the case of 4H-SiC, and here we have shown that it is delayed to above 7 MV/cm for 3C-SiC. The fact they both change failure mechanisms around 8.5 MV/cm makes the F-N tunnelling explanation not satisfactory. On the other hand, the electron impact ionization within the SiO_2 is determined by the oxide thickness and electric field. For the mostly studied ≈50 nm thick oxides of power MOS devices, the impact ionization is expected to occur at an electric field strength of ≈8 MV/cm [43, 44]. While for thin oxide layers, impact ionization occurs at higher electric fields, which also explains why even at a very high electric field of 15 MV/cm, a Weibull distribution can still be observed for the TDDB results of very thin (6-7 nm) SiO_2 layers on 3C-SiC [16]. As such, here we attribute mechanism III to the electron impact ionization.

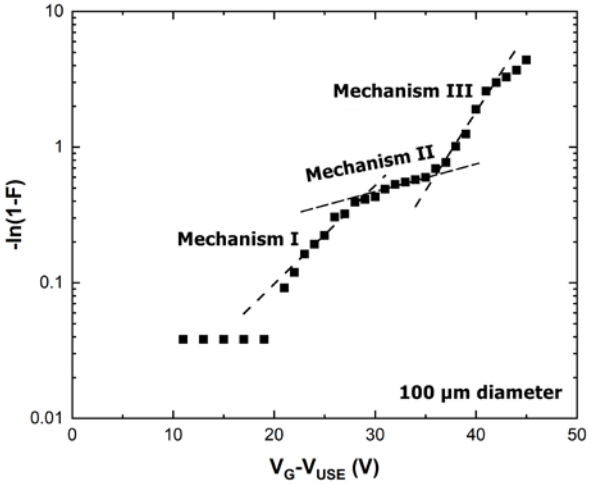

Fig. 5. Weibull distributions of Φ100 MOS capacitors as a function of applied gate bias, F is the failure rate and VUSE is the normal use voltage.

The three failure mechanisms can be more easily distinguished for Φ100 MOS capacitors by plotting -ln(1-F) against V_G-V_{USE} as shown in Fig. 5. F is the failure rate and V_{USE} is the nominal voltage of the device. Since the normal operating electric field of MOS devices is typically 3 MV/cm [4, 8], here we assume a V_{USE} of 20 V. An exponential function [45] described by Eq. (2) can be used to fit the three mechanism regions as seen in Fig. 5.

$$-\ln(1-F) = a \cdot e^{b(V_G - V_{USE})} \tag{2}$$

a and b are the fitting parameters. By multiplying a by 10^6, the maximum failure parts per million (PPM) of the Φ100 MOS capacitors working for 1 hour at 3 MV/cm and room temperature can be estimated. With the low field being dominated by mechanism I, the failure rate can be estimated to be around 3450 PPM, which is close to the latest 4H-SiC MOSFET results of 4100 PPM [45]. Although the 4H-SiC MOSFETs were tested at a higher temperature (150 °C) and a longer gate bias (168 h), the channel length of these commercial MOSFETs usually goes down to 1 µm [46], namely 10-100 times smaller gate active area than the Φ100 MOS capacitors studied here. Extrapolation from the high field (>8.5 MV/cm) data points suggests a much lower failure rate of 40 PPM, indicating a great room for further improvements if mechanism I can be minimized by improving material quality.

D. TDDB

Long-term TDDB test was performed on Φ100 MOS capacitors at room temperature using a custom-built dielectric breakdown rig. Gate leakage currents of up to 32 devices were monitored simultaneously in parallel, and the maximum current level was separately limited to 1 µA by series connected resistors. Any device with a gate leakage increasing to above 1 µA was removed from operation to protect the adjacent devices. Literatures have suggested that the thick gate oxide breakdown is a "weakest link" type of problem [8, 47, 48], thus can be described by the Weibull distribution expression as below:

$$F(T_{BD}) = 1 - e^{[-(\frac{T_{BD}}{t_{63\%}})^{\beta}]} \tag{3}$$

where T_{BD} is the TDDB running time, $t_{63\%}$ is the characterisitc time when 63% of all tested devices fail, and β is the Weibull slope, which is an indicator of failure mechanism variance between devices and should increase with reducing number of

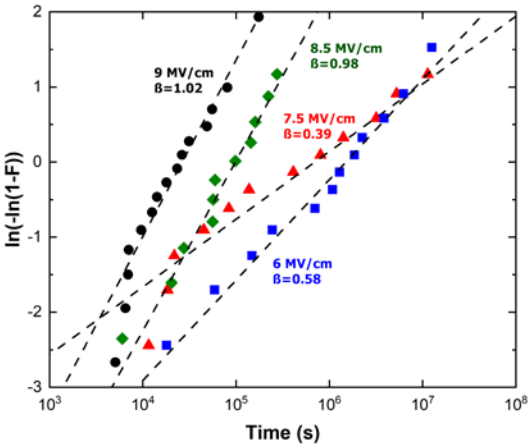

Fig. 6. Weibull distributions of devices failures at various electric fields on Φ100 MOS capacitors, obvious premature failures have been removed.

mechanisms.

Measurements were taken for 6 MV/cm, 7.5 MV/cm, 8.5 MV/cm and 9 MV/cm, and the Weibull distributions are shown in Fig. 6 with obvious premature failure tails removed. Even at high electric fields above 8.5 MV/cm, the extracted β values are still very low ≈1, an order of magnitude smaller than the values reported for 4H-SiC [7], suggesting that mechanism II may still be working behind the scene at such high fields. It can be seen in Fig. 6 that, the slope β for 9 MV/cm and 8.5 MV/cm are almost the same (≈1), whereas considerably reduced to 0.39 for 7.5 MV/cm. From previous discussions, we know it is because of the change of dominating failure mechanism from II to III with elevated electric fields. Further reducing the test field to 6 MV/cm confirmed an increase of β to 0.58 due to mechanism I, agreeing with the medium-term distribution analysis.

To project the lifetime of the fabricated MOS capacitors, $t_{63\%}$ is plotted against the applied gate electric field (the E model

[49]) as seen in Fig. 7. The field acceleration parameter is extracted to be 0.906 dec/ (MV/cm) for 7.5-9 MV/cm. From the projection, the lifetime of these devices can reach 10 years at room temperature with a maximum operating electric field of 4.5 MV/cm as shown in Fig. 7. As is known, temperature has a significant impact on the SiO2 life time. Although the testing rig is limited to room temperature, higher temperature performance of these MOS capacitors can still be estimated using the Arrhenius model $t_{63\%} \propto exp(E_a/kT)$, where E_a is the thermal activation energy. 3C-SiC MOSFETs operating at 300 °C had been demonstrated [36], but there were no reports on the E_a value. From the Al gated 4H-SiC MOS capacitor results [50], 0.5 eV was assumed for these 3C-SiC devices, and the life time projection for 150 °C is shown in Fig. 7. The predicted critical electric field required for 10 year life time drops considerably to 1.4 MV/cm at 150 °C, much lower than the 4H-SiC MOS capacitors results, ≈6 MV/cm [8]. However, it should be noted that, due to a positively charged 3C-SiC MOS interface as mentioned before, a forward gate bias accumulates more electrons at the 3C-SiC/SiO_2 interface at room temperature compared with the 4H-SiC case. As such, the actual temperature effects may be smaller than predicted in Fig. 7.

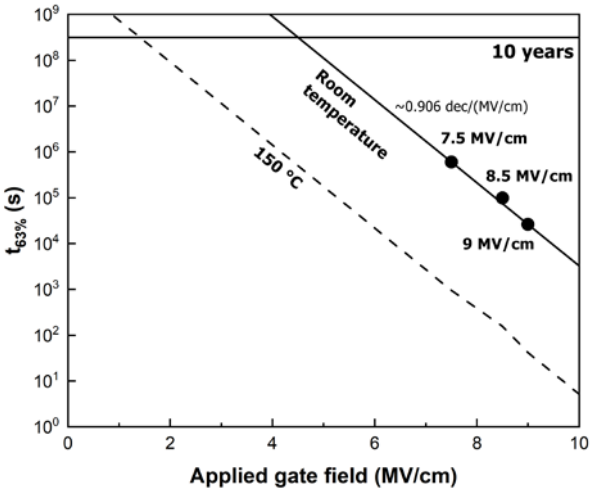

Fig. 7. Time to breakdown as a function of the applied electric field of Φ100 MOS capacitors and the projection of lifetime using the E model.

IV. Summary

A reliability study has been thoroughly performed on 3C-SiC MOS capacitors at room temperature, including leakage current evaluation, medium-term constant voltage and long-term TDDB tests. The effective barrier height at 3C-SiC/SiO_2 is experimentally obtained as very close to the theoretical value of 3.7 eV, and the F-N tunnelling is found to be dominating the gate leakage current only above a relatively high electric field of ≈7 MV/cm. According to the medium-term reliability test at a wide electric field range, an acceptable failure rate of 3450 PPM (1 hour at 3 MV/cm, room temperature) for the 100 µm diameter MOS capacitors is obtained, which can be further reduced to 40 PPM if the extrinsic defects (mechanism I) are neglected. Long-term TDDB tests over several months have been done for Φ100 MOS capacitors at 7.5 MV/cm, 8.5 MV/cm and 9 MV/cm. The field acceleration factor is found to be ≈0.906 dec/(MV/cm) in the studied range. Both the medium-term and long-term tests show a failure mechanism change of these MOS capacitors at 8.5 MV/cm, which is most likely caused by the impact ionization of electrons rather than the F-N tunnelling. Although the fabricated MOS capacitors are still suffering from a high number of extrinsic defects and further improvements are required, the projected lifetime is still remarkable and can reach 10 years, at 4.5 MV/cm and room temperature.

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